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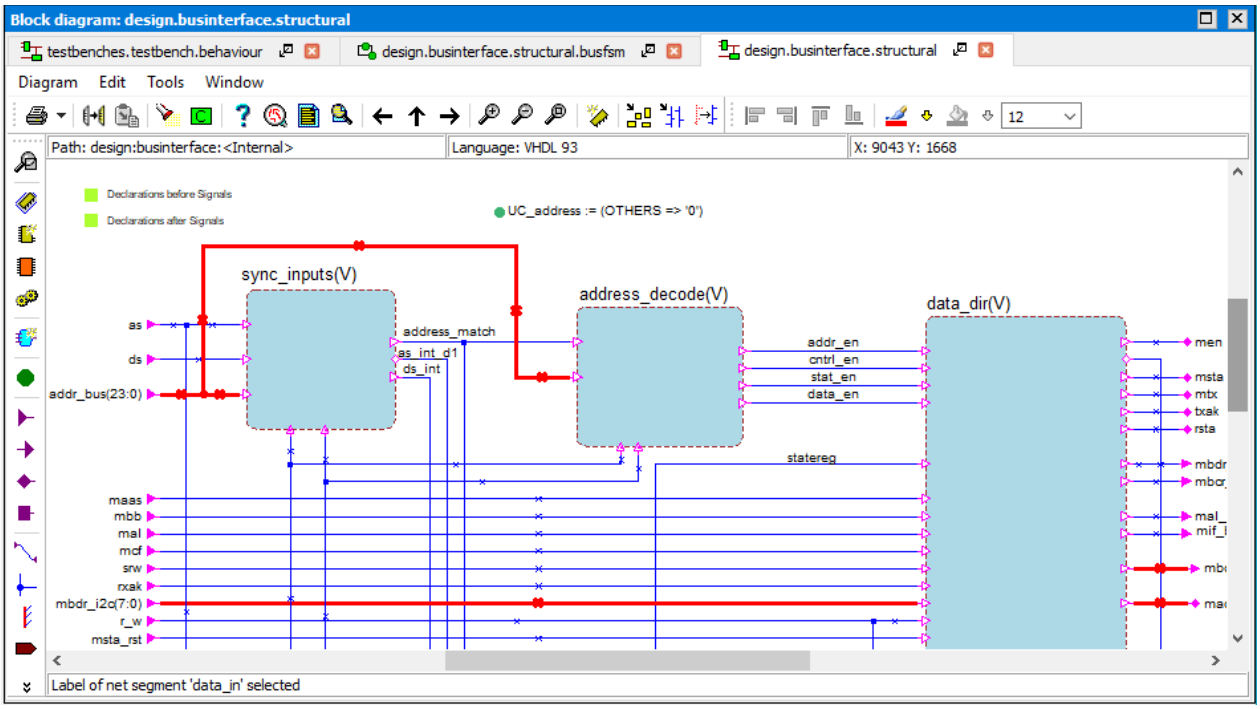
Ease 9.0 Release Notes

Introduction

Welcome to Ease 9.0. In this document we will give a brief overview of the changes in Ease 9.0. There was only one minor change to the database format (as a result of a bug fix), however we did not update the database number. The change we made is already supported in Ease 8.4 Revision 4 (but not in earlier revisions). This means that you will be able to a load projects saved using Ease 9.0 in Ease 8.4 Revision 4 (and later).

Even though we have tested all changes, we strongly recommend you make a backup of your projects before using it with Ease 9.0.

Multiple diagram editors open at the same time

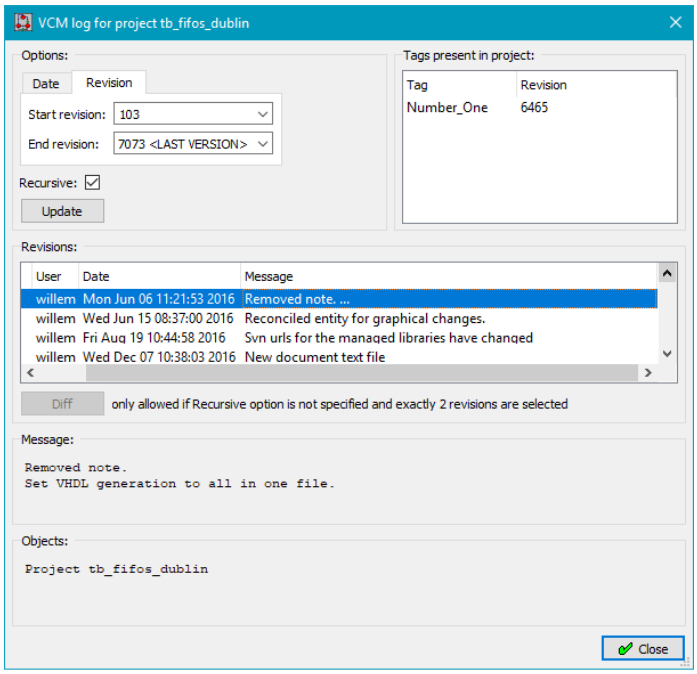


In Ease 9.0 it is possible to have multiple editor windows (and of different types) open at the same time. By default they will be shown as tab pages in the editor, but it is possible to undock the tab pages so you can place them in any way you like (e.g. side by side or on different monitors). When you open a diagram from the browser, and this diagram is not yet open in an existing editor, a new editor window will be opened. When you navigate to another diagram inside an existing editor window, you will remain within this editor. It is possible to have the same diagram open in multiple windows.

When an editor window is detached from the main window it will show its own search, lint and verify tabs.

Improved VCM revision log

It is now possible to select the begin and end date (or first and last revision) to be shown in the log window. The log entries are now shown in table view with 3 columns: user who performed the commit, commit date and the message (abbreviated to single line). The full message and the objects to which this message refer are at the bottom on the log.



Improved VCM performance

When performing VCM actions on multiple objects in the same library the actions will be bundled to reduce the number of client/server actions.

After some of the VCM actions (like commit for a library units inside one library) we now perform an incremental (partial) reload instead of a full project reload.

HDL Improvements

Generate statements can use attributes of signals to define the for-loop range.

When using VHDL direct instantiations the architecture to use can be specified for each component.

VHDL import now supports package declarations/bodies inside an entity declaration.

Added an option to the entity properties dialog to not generate VHDL USE clauses for instantiations of the entity. Sometimes needed when using pre-compiled libraries (e.g. provided by Xilinx).

Other new features

- Id 396: Graphical indication for ports on sensitivity list
- Id 615: Added 'Disconnect' entry to the port context menu to make it possible to manually route an un-routed port that is connected to a partially routed net.
- Id 1377: place diagram port immediately beside block port (if net has only 2 connected objects).

  Available from block port context menu 'Place opposite port' or using key sequence 'P, O'.

  Deprecated ‘P’ as shortcut to add a parameter in Verilog: use key sequence

‘A’, ‘P’ instead.

- Id 1378: block diagram editor, deprecated 'U' as shortcut to add an open tag.

  Use key sequence 'A', 'U' to add an open tag. 'U' is now used as first character in key sequence used for Update ('U', 'M' => Update from marker).
- Id 1687: incremental reload after VCM actions. Supported for objects of type entity, user context, user package, virtual package and text files. If the VCM action contains objects of another type a full reload will take place.
- Id 1745: A simple way to add 0, '0' or (OTHERS => '0') to a constant value tag.

  Use key sequence ‘A’, ‘0’ or ‘A’, ‘1’.
- Id 1786: allow constant value tag on bus rippers
- Id 1821: when copying a port using drag + SHIFT key, Ease will change the direction of the port being copied. This now also works for ports that have a virtual record type (the direction of all elements will be toggled).
- Id 1828: VCM status verification log now uses a list view instead of a tree view.
- Id 1829: Entries in VCM status verification log now have a tooltip with revision information.
- Id 1836: Option to disable verify/lint/HDL gen for an entity
- Id 1842: When creating a new tag the list of existing tags is now ordered by version number and the tag for the last version is selected.
- Id 1860: Improved the way the user can specify how VHDL instantiations should be generated. Use consistent settings in project, library and entity properties dialog.

For a complete list of bug fixes please refer to the support page on our web-site at:

https://www.hdlworks.com/support/ease/ease90.html

Supported platforms

- Windows (64 bit) 7 / 8.1 / 10
- Linux (64 bit, any recent distribution)

Licensing

EASE 9.0 uses Flexlm version 11.14.1.2 and requires a license daemon which is also 11.14.1.2 or later. Customers with a valid floating license must use this version or a newer version. Only the HDL Works daemon is required to be version V11.14.1.2 or later.
All older versions of EASE work with this new license daemon.