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Ease 9.2 Release Notes

Introduction

Welcome to Ease 9.2. In this document we will give a brief overview of the changes in Ease 9.2. For some of the new features we needed to make changes to the database format. This means that you will **not** be able to a load projects saved using Ease 9.2 in Ease 9.1 or before.

Even though we have tested all changes, we strongly recommend you make a backup of your projects before using them with Ease 9.2.

SystemVerilog

In EASE 9.2 we have made a start with supporting SystemVerilog. This release focusses around the synthesis functionality of the language. The internal SystemVerilog parser is fully compliant and can be set in 2005 and 2009 mode.

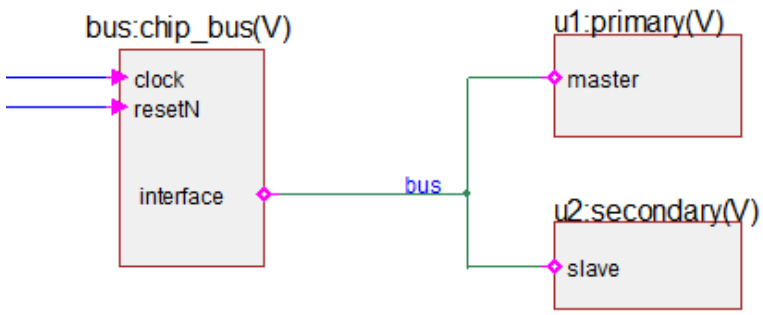
Verilog (all versions) are a part of the SystemVerilog language. There are some properties that apply to both Verilog and SystemVerilog.

The default language can be set to SystemVerilog in the project properties dialog.

SystemVerilog items for which EASE has a graphical representation in the database view are:

- Package
- Interface
- Program

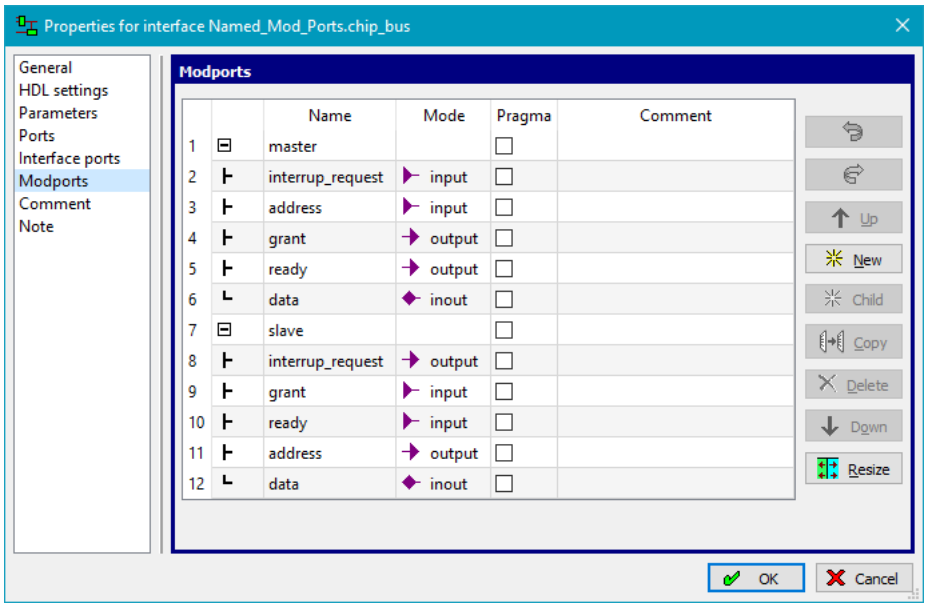
Packages and programs have text contents. User defined types can be declared in packages and used in interfaces, modules and programs. The type definition of nets and ports in those units is improved and the use of memory signals with a range and a dimension: like `[7:0]example[31:0]` is now supported.



Interface instantiation example

Packages can be used inside a module or interface using an import statement. The import statement is either placed before or inside the module or interface.

An ‘interface’ is a new SystemVerilog construct to encapsulate the communication information between Verilog modules. The contents of an interface can be a block diagram or a text file. A number of ‘modports’ can be defined on an interface. These ‘modports’ are used on other modules. An interface is instantiated like a module, but it has one special port named ‘interface’, which is always present on the instantiated interface. The interface port is used to connect to other ‘modports’ on instantiated modules. Ease supports the use of both named ‘modports’ and generic ‘interface ports’.



*F*igure 1: Modport definitions for an Interface

The net connected to the interface port of an interface instance is automatically named to the instance interface name.

Folder changes inside the project ‘.ews’ directory

The HDL file parts for text architectures, packages, processes and concurrent statement blocks are now located inside a folder named ‘ease.hdl’ (inside the <project>.ews)

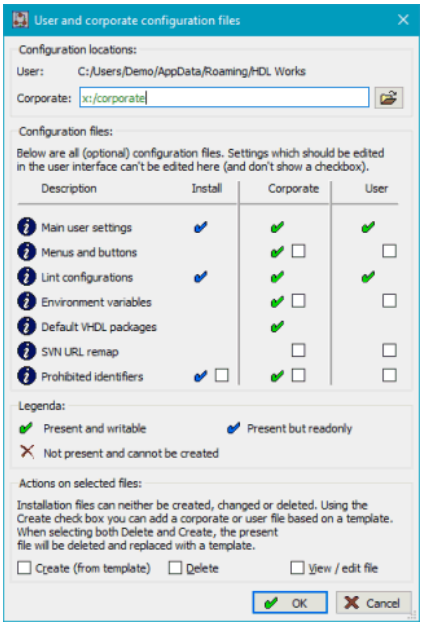
So a process file snippet is now in:

`<ease.hdl>/<library/<entity>/<architecture>/process.vhd`

New text files (including Verilog include files and other internal HDL files) will now be placed inside `<project>.ews/ease.hdl/` folder.

This reduces the amount of folders present in the <project>‘.ews’ folder.

User and corporate location dialog



EASE can use a number of configuration files, which can reside in the user or corporate location.

To simplify the use of these configuration files and show which files are present a new 'User and corporate configuration files dialog' is used.

The dialog allows you to setup (create/edit/delete) configuration files for which no user interface is present. New files are created using a template from the installation showing you the required format.

Lint

A number of new lint checks have been added to EASE:

- OS4: VHDL lint check for integer/natural/positive signals without a range constraint.
- OS5: Only use rising edge clock.
- OS6: Avoid using shared variables.
- CP14: VHDL CP14 lint check now also checks for unused enumerated values for enumerated types declared inside architectures.
- Misc 16: prohibit use of reserved identifiers (like Verilog keywords in VHDL and vice versa).
- Misc17: only allow generics and ports inside an entity

Other new features

- New user and corporate configuration dialog
- Function key 'F9' can be used to resize dialog tables
- Example projects are stored as a single file and can be expanded to a directory of choice
- Id 1801: Allow double click on an object to edit its properties
- Id 2026: Easy way to connect selected ports using CBN tags
- Keep tooltip open when left mouse is down, but outside tooltip window
- Contents of a tooltip can be copied to the clipboard using the <Ctrl-C> key
- Added search dialog to the HDL text editor in dialogs
- In the browser show full entity context menu for external entities if they are shown as part of the HDL file they belong to

For a more complete list (including bug fixes) please refer to the support page on our web-site at:

https://www.hdlworks.com/support/ease/ease92.html

Supported platforms

- Windows (64 bit) 8.1 / 10
- Linux (64 bit, any recent distribution)

Licensing

Ease 9.2 uses FlexNet Publisher (FLEXlm) version 11.14.1.2 and requires a license daemon which is also 11.14.1.2 or later. Customers with a valid floating license must use this version or a newer version. Both the FLEXlm daemon and the HDL Works daemon are required to be version 11.14.1.2 or later.
All older versions of Ease work with this new license daemon.

You can download the latest license daemons here:

https://www.hdlworks.com/downloads/flexlm.html